VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY,BURLA

RESULT OF 1ST SEMESTER (M.TECH) EXAMINATION NOVEMBER 2016 (GRADE LIST)

BRANCH :ELECTRONICS & TCE (VLSI SIGNAL PROCESSING)

1ST SEMESTER		SUBJECTS->	DVLSID	VLSIT	SDM	AVLD	ASP	VLSIDLAB-I	VLSITLAB	SEMN-I	CVV-I	SGPA	CGPA
SL	REG N0.	NAME CREDIT->	04	04	04	04	04	02	02	02	02		
1	1605070021	P MRUTYUNJAYA DAS	A	A	C	C	B+	A	A+	O	A+	7.29	7.29
2	1605070022	SATYA NARAYAN PANIGRAHI	A	B+	B	B	A	A+	A+	A+	A	7.50	7.50
3	1605070023	PIYUSH KAR	A+	A+	A	A+	A+	O	A+	O	O	9.07	9.07
4	1605070024	AMIT KUMAR JHA	A	B+	B+	B	B+	A+	A+	A+	O	7.64	7.64
5	1605070025	SUSANTA KUMAR SAMAL	B+	C	P	F	B	B+	A	A	B+	*.**	*.**
6	1605070026	ABHISHEK KUMAR DIWAKAR	A+	A+	B	B+	B+	A+	A+	A+	A+	8.00	8.00
7	1605070027	PRITAM NANDA	F	AB	AB	AB	F	F	F	F	AB	*.**	*.**
8	1605070028	RASHMISHREE ROUT	A	A	C	B	A	A+	A+	A+	A+	7.57	7.57
9	1605070029	SWETA PADMA BHOI	B+	B	C	B	B+	A+	A	A+	A	6.86	6.86
10	1605070030	APARAJITA SAHU	B+	B	C	C	C	A	A+	O	A+	6.57	6.57
11	1605070031	ANJALI RAY	O	A	A+	A	A+	O	A+	O	O	9.07	9.07
12	1605070032	ARPITA KAR	B+	B+	C	C	B+	A	A	O	A	6.86	6.86
13	1605070033	RITUPARNNA PUJARI	B+	B	F	F	A	B+	A	A	B+	*.**	*.**
14	1605070034	APARNA SHIT	B+	B	P	F	B+	B+	A	A	A	*.**	*.**

WH* - Withheld due to Other reason

DVLSID-->DIGITAL VERY LARGE SCALE INTEGRATION DESIGN

VLSIT-->VERY LARGE SCALE INTEGRATION TECHNOLOGY

SDM-->SEMICONDUCTOR DEVICE MODELING

AVLD-->ANALOG VLSI DESIGN

ASP-->ADVANCED SIGNAL PROCESSING

VLSIDLAB-I-->VERY LARGE SCALE INTEGRATION DESIGN LAB.-I

VLSITLAB-->VLSI TECHNOLOGY LABORATORY

SEMN-I-->SEMINAR-I

CVV-I-->COMPREHENSIVE VIVA VOCE-I

(CONTROLLER OF EXAMINATIONS)